UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,885	03/18/2004	Haruhiko Murata	Q80543	5201

23373 7590 04/22/2005

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,885	MURATA ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04282004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation, *"wherein said platinum-metal based electroless plated layer is an electroless Pd-plated layer,"* is unclear. Examiner is unsure as to meaning. Correction and/or clarification is required.

Claim Rejections – 35 U.S.C. 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 7, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fey et al. in view of Chow et al. ("Surface Properties and Solderability Behaviour of Nickel-Phosphorous and Nickel-Boron Deposited by Electroless Plating," Surf. Interface Anal. Vol. 31, (2001), pp. 321 – 327).

5. Regarding Claims 1 and 2, Fey et al. disclose a wiring board comprising:

a wiring laminate portion including dielectric layers (14a,14b) (Figure 1) containing a polymeric material (Col. 6, lines 63 – 67) and conductor layers (12) (Col. 5, lines 9 – 14) laminated alternately so as to form a first main surface out of one of said dielectric layers, and

a plurality of metal terminal pads (40) (Figure 2) disposed on said main surface, wherein

each of said metal terminal pads has a structure in which a Cu-plated (electrodeposited) layer (28) is deposited on a side of said first main surface and a Au-plated layer (64) (Figure 9) is disposed in an outermost surface layer portion of said metal pad, while an electroless Ni-plated layer (62) is disposed as a barrier layer between the Cu- plated layer and said Au-plated layer (Col. 9, lines 35 – 41).

Fey et al. do not disclose that the electroless Ni-plated layer has a P content not higher than 3 percent by weight. Chow et cal.disclose the use of commercially available (Shipley Ronal) materials (Table 1, p.322) with a 2 – 4 wt. % P content for improving adhesion to Cu films (p. 327, left side, Surface Morphology Studies, 1st para.). It would have been obvious to one of ordinary skill in the art at the time of the invention to use Chow et al. in forming an improved film of increased adhesion and solderability in Fey et al.

6. Regarding Claim 3, Fey et al. do not disclose that the electroless Ni-plated layer is a Ni-B based electroless layer. Chow et cal.disclose the use of commercially available (Shipley Ronal) materials (Table 1, p.322) with a 0.25 wt. % B content for improving adhesion to Cu films (p. 327, left side, Surface Morphology Studies, 1st para.). It would have been obvious to

one of ordinary skill in the art at the time of the invention to use the procedures of Chow et al. in forming an improved film of increased adhesion and solderability in Fey et al.

7. Regarding Claim 4, Fey et al. disclose that the electroless nickel-plated layer (62) is in direct contact (Figure 9) with the Au-plated layer (64) made of electroless Au (Col. 8, lines 37 – 41).

8. Regarding Claim 5, Fey et al. do not disclose that the thickness of the electroless Ni-plated layer is in the range, 2 to 7 um and the thickness of the Au-plated layer is in the range, 0.03 to 0.1 um. Parameters such as contact layer thickness in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired electrical resistances. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate thicknesses of layers within the ranges as claimed in order to form a contact of reduced resistance.

9. Regarding Claims 6 and 7, Fey et al. disclose a wiring board comprising

a wiring laminate portion including dielectric layers (14a,14b) (Figure 1) containing a polymeric material (Col. 6, lines 63 – 67) and conductor layers (12) (Col. 5, lines 9 – 14) laminated alternately so as to form a first main surface out of one of said dielectric layers, and

a plurality of metal terminal pads (40) (Figure 2) disposed on said main surface, wherein

each of said metal terminal pads has a structure in which a Cu-plated (electrodeposited) layer (28) is deposited on a side of said first main surface and a Au-plated layer (64) (Figure 9)

is disposed in an outermost surface layer portion of said metal pad, while a platinum metal based electroless plated layer (62) is disposed as a barrier layer between the Cu- plated layer and said Au-plated layer (Col. 6, lines 11 – 15) (Col. 8, lines 30 – 37).

10. Regarding Claim 9, Fey et al. disclose that an electroless Pt-plated layer (Col. 8, 30 – 37) (Col. 6, lines 11 – 15) is present.

11. Regarding Claim 10, Fey et al. do not disclose that the thickness of the platinum-metal-based electroless plated layer is in the range, 0.05 – 1 um. Parameters such as contact layer thickness in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired electrical resistances. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate thicknesses of layers within the ranges as claimed in order to form a contact of reduced resistance.

12. Claims 11 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fey et al., in view of Chow et al., as applied to Claims 1 – 4, 6, 7, 9.and 10, and further in view of Bengston et al. (5,235,139).

13. Regarding Claims11 – 13, Fey et al. disclose a wiring board comprising:

a wiring laminate portion including dielectric layers (14a,14b) (Figure 1) containing a polymeric material (Col. 6, lines 63 – 67) and conductor layers (12) (Col. 5, lines 9 – 14) laminated alternately so as to form a first main surface out of one of said dielectric layers, and

a plurality of metal terminal pads (40) (Figure 2) disposed on said main surface, wherein each of said metal terminal pads has a structure in which a Cu-plated (electrodeposited) layer (28) is deposited on a side of said first main surface and a Au-plated layer (64) (Figure 9) is disposed in an outermost surface layer portion of said metal pad.

Fey et al. do not disclose the presence of an Ni-P based electroless layer in contact with the underlying Cu layer and a P-barrier electroless metal plated layer for blocking or suppressing P-diffusion from said Ni-P based electroless Ni-plated layer to said Au-plated layer, wherein the P-barrier layer is disposed between the Ni-P based electroless Ni-plated layer and the Au layer.

Fey et al. do disclose that the noble metal layer (60) (Figure 6) may be two layers (Col. 8, lines 35 – 37), followed by an electroless Au layer (Col. 9, line 41). Bengston et al. disclose the formation of a two layer structure wherein an electroless Ni-B layer (24) (Figure 1C) is formed, followed by an electroless Ni-P layer (26) (Col. 6, lines 50 – 55) where the Ni-B based electroless Ni-plated layer is a P-barrier electroless metal plated layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to rearrange the electroless Ni plated layer sequence in Bengston et al. to obtain a Au/Ni-B/Ni-P/Cu structure to reduce interdiffusion and to combine Bengston et al. with Fey et al. to produce an efficient and reliable bond pad.

14. Regarding Claim 14, Fey et al. disclose that the layer of metal (Col. 6, lines 13 – 15) (Col. 8, lines 35 – 37) formed as a P-barrier layer is an electroless plated Pt layer.

15. Regarding Claim 15, Fey et al. do not explicitly disclose that the Au-plated layer is made of an electroless reduction Au-plated layer. Bengston et al.disclose the use of an electroless Au layer formed by a reduction procedure (Col. 7, lines 45 – 59). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Bengston et al. with Fey et al. to obtain a high purity Au layer over the Ni alloy layer (Bengston et al., Col. 7, lines 48 – 49)

16. Regarding Claim 16, Fey et al. do not disclose that the thickness of the electroless Ni-P-based plated Ni layer is in the range, 2 to 7 um and the thickness of the P-barrier electroless Ni-plated layer is in the range, 0.05 to 2 um. Parameters such as contact layer thickness in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired electrical resistances. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate thicknesses of layers within the ranges as claimed in order to form a contact of reduced resistance.

17. Claims 17 – 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fey et al. in view of Bengston et al.

18. Regarding Claims 17 and 18, Fey et al. disclose a wiring board comprising:

a wiring laminate portion including dielectric layers (14a,14b) (Figure 1) containing a polymeric material (Col. 6, lines 63 – 67) and conductor layers (12) (Col. 5, lines 9 – 14) laminated alternately so as to form a first main surface out of one of said dielectric layers, and

a plurality of metal terminal pads (40) (Figure 2) disposed on said main surface, wherein

each of said metal terminal pads has a structure in which a Cu-plated (electrodeposited) layer (28) is deposited on a side of said first main surface and a Au-plated layer (64) (Figure 9) is disposed in an outermost surface layer portion of said metal pad.

Fey et al. do not disclose the presence of a layer containing an Ni-B based electroless Ni-plated layer in contact with the underlying Cu layer and a Ni-P-based electroless Ni-plated layer disposed between the electroless Ni-B layer and the Au layer.

Fey et al. do disclose that the noble metal layer (60) (Figure 6) may be two layers (Col. 8, lines 35 – 37), followed by an electroless Au layer. (Col. 9, line 41). Bengston et al. disclose the formation of an electroless nickel alloy (Ni-B) layer on Cu (Col. 6, lines 50 – 55) wherein the Ni-B layer is used as a barrier layer to reduce P diffusion into the overlying Au layer. This is followed by an electroless Ni-P layer between said Cu-plated layer and said Au-plated layer, It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Bengston et al.with Fey et al. to obtain electroless layers of Ni-P/Ni-B/Cu to reduce interdiffusion (Fey et al., Col. 1, lines 31 – 35),

Further, Fey et al. do not disclose that the Ni-P layer is thinner than the Ni-B layer. Parameters such as contact layer thicknesses in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired electrical resistances. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate thicknesses of layers within the relative ranges as claimed in order to form a contact of reduced resistance.

19. Regarding Claim 19, Fey et al. do not disclose that the Ni-P based electroless metal plated layer is not thicker than 2 um. Parameters such as contact layer thickness in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired electrical resistances. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate thicknesses of layers within the range as claimed in order to form a contact of reduced resistance.

20. Regarding Claim 20, Fey et al. do not explicitly disclose that the Au-plated layer is made of an electroless reduction Au-plated layer.Bengston et al.disclose the use of an electroless Au layer formed by a reduction procedure (Col. 7, lines 45 – 59). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Bengston et al. with Fey et al. to obtain a high purity Au layer over the Ni alloy layer (Bengston et al., Col. 7, lines 48 – 49).

21. Regarding Claim 21, Fey et al. do not disclose that the thickness of the electroless Ni-B-based plated Ni layer is in the range, 2 to 7 um and the thickness of the Ni-P based electroless layer is in the range, 0.05 to 2 um. Parameters such as contact layer thickness in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired electrical resistances. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate thicknesses of layers within the ranges as claimed in order to form a contact of reduced resistance.

22. Claims 22 – 24, and 26 – 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fey et al. in view of Chow et al., as applied to Claims 1 – 7, 9, and 10, and further in view Lee ("Lead-Free Chip Scale Soldering of Packages," Chip Scale Review, (March – April, 2000), pp. 1 - 6).

23. Regarding Claims 22 – 24, and 26 –28, Fey et al. do not disclose the presence of solder balls so that said metal terminal pads are to be connected to mother board side terminal pads through said solder balls. However the connection of wiring boards to other elements through solder balls at pad areas is well established in the art. Lee, for example, discloses (p.2, para. 4 - 9) the use of improved solder connections on wiring boards. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Lee with Fey et al. to provide a reliable interconnected wiring board and external element.

Further, Fey et al. do not disclose an SnAg alloy whose liquidus is not lower than 200 C. Lee discloses Sn Ag alloy (Table 1) with liquidus temperatures in excess of 200 C . It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Lee and Fey et al. to obtain solder connection areas of improved strength and compatibility with conductive pads.

24. Claims 25 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fey et al. in view of Chow et al., as applied to Claims 1 – 7, 9, and 10, and further in view of Hwang et al. (Effects of Pb Contamination on the Material Properties of Sn/Ag/Cu Solder, "

Chip Scale Review (January – February 2001), pp. 1 – 5).

25. Regarding Claims 25 and 29, Fey et al. do not disclose the presence of solder balls containing Sn alloy and a lead concentration not higher than 5%..Hwang et al. discloses Sn solder alloys having Pb concentrations introduced at levels below 5 % to provide comparative data on properties, wherein no significant changes were detected at low concentrations. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Hwang et al. with Fey et al. to obtain a low Pb concentration solder for improved wettability and reliability.

26. Claims 30 – 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fey et al. in view of Chow et al., as applied to Claims 1 – 7, 9, and 10, and further in view of Lee.

27. Regarding Claims 30 – 32, as discussed above for Claims 22 – 24 and 26 –28, Fey et al. do not disclose the presence of solder balls so that said metal terminal pads are to be connected to mother board side terminal pads through said solder balls. However the connection of wiring boards to other elements through solder balls at pad areas is well established in the art, as for example, disclosed by Lee above. Further, Fey et al. do not disclose an SnAg alloy whose liquidus is not lower than 200 C. Lee discloses Sn Ag alloy (Table 1) with liquidus temperatures in excess of 200 C. The rejection is essentially the same as presented for the previous claims.

28. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fey et al. in view of Chow et al.and Lee, as applied to Claims 1 – 7, 9, 10, and 30 – 32, and further in view of Hwang et al.

29. Regarding Claim 33, as discussed above, Fey et al. do not disclose the presence of solder balls containing Sn alloy and a lead concentration not higher than 5%..Hwang et al. discloses Sn solder alloys having Pb concentrations introduced at levels below 5 % to provide comparative data on properties, wherein no significant changes were detected at low concentrations. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Hwang et al. with Fey et al. to obtain a low Pb concentration solder for improved wettability and reliability.

30. Claims 34 – 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fey et al. in view of Lee.

31. Regarding Claims 34 – 36, as discussed above for Claims 22 – 24 and 26 –28, Fey et al. do not disclose the presence of solder balls so that said metal terminal pads are to be connected to mother board side terminal pads through said solder balls. However the connection of wiring boards to other elements through solder balls at pad areas is well established in the art, as for example, disclosed by Lee (discussed above). Further, Fey et al. do not disclose an SnAg alloy whose liquidus is not lower than 200 C. Lee discloses Sn Ag alloy (Table 1) with liquidus temperatures in excess of 200 C. The rejection is essentially the same as presented

for the previous claims.

32. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fey et al. in view of Bengston et al., Smith and Lee, as applied to Claims 17 – 21, and 34 –36, and further in view of Hwang et al.

33. Regarding Claim 37, the rejection is identical to that presented for Claim 33 above.

Conclusions

34. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
April 16, 2005

EDDIE LEE
SUPERVISORY PATENT EXAMINER